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Sheet 2 of 2

Complete if Known	
Application Number	09/851,622
Filing Date	May 8, 2001
First Named Inventor	Ejaz Ul Haq
Group Art Unit	2816
Examiner Name	~~Unassigned~~ David Lo
Attorney Docket Number	44176.00033

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
DL	1	"IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)", IEEE Std. 1596.3-1996, March 21, 1996, XP-002106653, Introduction, Contents and pages 1-30.	
DL	2	4M x 18 SLDRAM Preliminary Data Sheet 9/97 from SLDRAM Consortium.	
DL	3	1M x 16Bit x 4 BANKS DDR SDRAM (Rev. 0.5 June 1997) from Samsung.	
DL	4	Kim, et al. "A 640MB/s Bi-Directional Data Strobed, Double-Data-Rate SDRAM with a 40mW DLL Circuit for a 256MB Memory System", ISSCC98 Digest, pp. 158-159, February 6, 1998.	
DL	5	Morooka, et al. "Source Synchronization and Timing Vernier Techniques for 1.2GB/s SLDRAM Interface", ISSCC98 Digest, pp. 160-161, February 6, 1998.	
DL	6	Lau, et al. "A 2.6 GB/s Multi-Purpose Chip-to-Chip Interface", ISSCC98 Digest, pp. 162-163, February 6, 1998.	
DL	7	LVDS I/O (Scalable Coherent Interface Documents) IEEE P1596.3 working-group activity for high-speed signal link interface, 3 pages.	
DL	8	Hyper-LVDS I/O Cells (LSI Logic Product Briefs), 2 pages.	
DL	9	Crisp, Richard, "Direct Rambus Technology: The New Main Memory Standard", November/December 1997 issue of IEEE Micro.	
DL	10	Direct RDRAM 64/72-Mbit (256Kx16/18x16d), "Advance Information" of 64M/72M Direct RDRAM Data Sheet, dated October 2, 1997.	
DL	11	Tamura, et al. "PRD-Based Global-Mean-Time Signaling for High-Speed Chip-to-Chip Communications", ISSCC98 Digest, pp. 164-165 & pp. 430-432; February 6, 1998.	
DL	12	Griffin, et al. "A Process Independent 800MB/s DRAM Bytewide Interface Featuring Command Interleaving and Concurrent Memory Operation", ISSCC98 Digest, pp. 156-157, February 6, 1998.	
DL	13	RamLink, LVDS I/O (Scalable Coherent Interface Documents) IEEE P1596.4 working-group activity for high-speed signal link interface, 3 pages.	
DL	14	XILINX® Application Note: "Using the Virtex SelectIO", XAPP 133 October 21, 1998 (Version 1.11), 12 pages.	
DL	15	Rambus®, "Rambus® Technology Overview, including Introduction and The Rambus Solution, Copyright February 1999, last modified: February 12, 1999, 5 pages.	

Examiner Signature		Date Considered	10/4/01

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